ADVANCED DIGITAL PROCESSOR RESEARCH AT DREA

by

D.V. Crowe
Defense Research Establishment Atlantic
Dartmouth, Nova Scotia, Canada

This informal presentation deals with an array processor built by ESE Ltd of Toronto under contract to the Defense Research Establishment Atlantic, Dartmouth, Nova Scotia, Canada. The processor and software was delivered to DREA in August, 1979 for a brief evaluation period.

The hardware of the processor is configured around arithmetic units (AU) running at 8 MHz. These AU's perform complex floating point arithmetic. The AU's operate with cache memory and can be configured in groups of 2,4,6 or 8. The system that was built has 4 AU's and 128K of 40-bit main data memory. Main data memory has an address space of 8 Megawords and uses inexpensive MOS RAM memory. The entire processor is a synchronous machine and uses pipelining and memory interleaving to achieve 8 MHz throughput.

The control is divided-up among an arithmetic control unit, a data transfer control unit, an I/O control, and a supervisory controller. The instruction sets of both the ACU and TCU are designed to operate on large blocks of data with each instruction. Examples are (1) complex vector multiply with conjugation and add, and (2) an FFT butterfly pass with bit reversal addressing.

The software of the control supervisor schedules the running of the ACU and TCU according to assigned priorities of various tasks. A task might be programmed request from a networked computer, or a predefined task that is initiated by an interrupt (e.g., the arrival of new data). Interleaving of tasks is easily handled as a natural consequence of the design of the processor. Dynamic allocation of main data memory for tasks and intertask communication are possible with this operating system.

Currently software supports the standard vector and signal processing functions. In addition scalar operations and control structures for a demonstration program in the active sonar field has been completed.

The project engineer for this processor is R. Trider at DREA.

DISCUSSION

R. Seynaeve Will the processor you described be used in operational systems?

D.V. Crowe The processor will be included as the hardware part of an operational design program proposal for sonar.