THE MSP-3 AND THE SPS-81

by

John S. Padgett *
Naval Research Laboratory
Washington, D.C. 20375 USA

ABSTRACT

The Large Aperture Acoustics Branch of the Naval Research Laboratory has developed a sea-going signal processing system in which two different types of array processors are used - a Signal Processing Systems SPS-81 and several Computer Design and Applications MSP-3 array processors. This paper briefly covers the differences in the two processors and why we have used both types.

INTRODUCTION

For some years, the Large Aperture Acoustics Branch of the Naval Research Laboratory has been involved with recording and subsequent analysis of acoustic signals at sea. In the past year, we have assembled a sea-going signal processing system which will give us the advantages of less time to publication, better results (since analog recording will cause significant data distortion), and improved capability for monitoring the experiment.

When we selected the equipment to be used, we had to pay attention to portability, since the equipment would be used on several different ships, and flexibility of architecture, since the type of data analysis often varies considerably from one experiment to the next. These two constraints, in addition to the traditional values of cost, speed, and reliability, have led us to use multiple MSP-3 processors whenever possible and supplement these with an SPS-81 when necessary. Both types of array processors are interfaced to a DEC PDP-11/34.

This paper will attempt to describe the differences between the design philosophies of the processors and show how each processor fits our requirements. In addition, some general comments will be made based on our experiences (good and bad) with the processors.

---

* *Presented by J.M. Griffin, Naval Research Laboratory, U.S.*

1. Characteristics of MSP-3 and SPS-81

1.1 MSP-3 (manufactured by Computer Design and Applications, Inc.)

1.1.1 General Description

The MSP-3 is a two card array processor which plugs into two adjacent peripheral slots of a PDP-11 backplane. It is relatively inexpensive (under $14000), consumes 50 watts of power, and is about one third as fast as larger array proccessors (13 msec for 1024 point complex FFT). Programming is in PROM, so loading before running is neither required nor possible. Data is stored in 2K by 48 bit (24 real, 24 imaginary) internal RAM in block floating point format, and many operations (like FFT) auto-scale the data.

1.1.2 Hardware Structure

The MSP-3 has 2K complex RAM for data storage, 2K PROM for trig constants, and 1K of program PROM, in addition to various configuration registers and one 8 bit exponent register. Since programming requires PROM burning, the internal hardware will not be covered any further.

1.1.3 Interface to Host (PDP-11)

Interface to the host computer is through four registers: control and status, opcode, argument, and unibus address. Each operation requires the host to set up at least the first two registers, so the host has to do more work to keep the MSP-3 going than a larger array processor would require.

1.1.4 Software

Programs for the MSP-3 are all in PROM, so altering the internal programming is rather difficult. Library functions can be selected when the MSP-3 is purchased, and include such standard routines as complex FFTs up to 2K.

Since even the simpler functions, such as loading internal MSP-3 registers, typically require the host to load three MSP-3 interface registers, the host has to do a bit of work just to keep the MSP-3 running. This can be alleviated greatly by using the "micro-chainer" which lets the MSP-3 read its instructions from host memory and execute them. We have found this to be a great help when the host processor is heavily loaded.

1.2 SPS-81 (manufactured by Signal Processing Systems, Inc.)

1.2.1 General Description

The SPS-81 is a large 16 bit integer array processor which is essentially a fast mini-computer. It can hold up to 256K by 32 bits of its own bulk memory, and can be interfaced directly to peripherals like disks and A/Ds via the internal bus. Once the host computer starts it, the SPS-81 can process, access its own peripherals, and access host memory and peripherals with no further

host intervention. A 1024 point complex FFT takes 4.2 msec, and transform sizes up to 16K complex can be easily handled.

1.2.2 Hardware Structure

Internally the SPS-81 consists of three separate asynchronous processors: IOP (167 nsec) which controls the other two processors, accesses peripherals and host; IS (167 nsec) which sequences and controls the AS; and AS (500 nsec) which does complex integer arithmetic and can do an FFT butterfly in one instruction. The IOP consists of four identical but different priority "channels", where the highest priority channel not in a wait state will run. This provides a good way to have interrupts (for A/D, etc.) with no context switch time.

1.2.3 Interface to Host (PDP-11)

The SPS-81 has four "mode control registers" on the Unibus which enable the host to start, stop, or single step the 81. The registers and program memories are available to the host for loading or reading via a 4K "B-Bus" which appears on the host Unibus.

1.2.4 Software

The initial programming of an array function into SPS assembly language is quite difficult because of the complexity of the machine. Once this is done, future applications become easier because of an SPS software package called the "Executive Interpreter" which interprets and executes commands found in either host memory or in SPS bulk memory, depending on which version of the interpreter is used. The "Interpretive Command Language" (ICL) has 17 different commands available for modifying or reading SPS internal registers, running SPS assembly language routines, conditional GO-TO, etc. Loops and subroutines are easy to use in ICL and SPS registers can be used for counters, pointers, and data storage. This promotes flexibility and ease of programming without adding much overhead, since the ICL interpret-and-execute time is small compared to array operations like FFT.

2. Reasons for Using Each Type Processor

2.1 MSP-3

Since we cannot afford to hold up sea experiments for equipment repairs, we want to opt for the sea-going system that is most reliable, and which allows us a chance to continue partial processing in the event of equipment failure (graceful degradation). The MSP-3 is small, has low power consumption, and is approximately one-fifth the cost of a larger array processor like the SPS-81. If an MSP-3 fails at sea, we can usually continue processing if we process less signal lines or make other reductions. Furthermore, if processing requirements for a particular experiment can be met with just 2 or 3 MSP-3s, then we can take the number required plus 1 for spare and have a physically smaller system which consumes less power.

2.2 SPS-81

The SPS-81 is used when needed because of its speed, independence of host computer, and ability to work with large arrays. Multiple MSP-3s could overcome speed problems, but the host computer would have more work to do to keep them running. In addition, large arrays would be impractical to work with, since the operations would have to be done in steps.

3. Comments

3.1 MSP-3

The MSP-3s have been very reliable (except for some early firmware bugs), with only 1 failure of 5 units in about 8 months. Considering the number of times they have been pulled in and out of backplanes, and the shipping and sea duty they went through, this is perfectly acceptable. Programming is easy, but does load the host computer since the host has to initiate every function. This can be alleviated by the use of the previously mentioned micro-chainer. Program memory size (1K PROM) has been a headache to us, since we always have to compromise on which functions we want in our library.

Block floating point capability has caused a few extra programming steps. For our applications, we require time to frequency transforms for each hydrophone, then space to angle transforms for each selected frequency line. After the first FFT, all lines for one hydrophone will have the same block exponent, but all hydrophones for one line may not. Since the input to the beamformer requires all hydrophones for each line, the numbers have to be shifted to where they all have the same block exponent. This is not a problem with integer or full floating point format.

Power consumption (50 watts) of the MSP-3 is small compared to large array proccessors, but large enough to cause problems with power distribution. The PDP-11 backplanes cannot handle much more than that, so peripheral slots must be sparsely populated when MSP-3s are included.

One fringe benefit of the MSP-3 has been the assistance of the Computer Design and Applications sales representative, Andy Lukas, who has provided many excellent suggestions on using the MSP-3 for our applications.

3.2 SPS-81

Since the SPS-81 is a faster, much more complicated machine, it has been less reliable than the MSP-3, with several failures in the past 2 years. Unfortunately, many of the failures have been of a devious nature, where the machine kept running but the output began looking a little funny. For this reason, we strongly recommend either frequent running of diagnostics or running diagnostics as a background task.

In our applications, the integer nature of the 81 can cause problems. Improper scale settings can result in loss of data either through overflow (if looking at synthesized cw signals) or shifting down too far (if looking at noise).

We have had some problems in writing to the host computer with a Unibus release taking place before the write finishes. This can cause bad data to be written and/or corruption of unrelated areas of host memory. This can be avoided by doing a read after write (often unacceptable) or by waiting a "long" time before doing a Unibus release. Our complaint about this situation is that the hardware should take care of ensuring that Unibus accesses are done in a legal manner.

4. Conclusions

Whenever possible, we prefer to use many small array processors such as the MSP-3 for the advantages of lower power consumption, graceful degradation, and flexibility of architecture. However, we still have to occasionally use a larger processor such as the SPS-81 for its ability to handle large arrays and to run without host processor intervention.

DISCUSSION

H.J. Alker Are there any trace capabilities available for the MSP hardware?

J.M. Griffin The hardware has no trace capability. Microcode must be debugged using a simulator prior to burning the PROMS. The simulator does have a trace capability.

W.G. Wagner Does the SPS 81 have its own I/O interfaces?

J.M. Griffin Yes it does, and we have used it to interface to high-speed A/D systems just as other have with the MAP and FPS processors.

B. Pennoyer Have you increased the SPS 81 software library?

J.M. Griffin No, we have made only minor variations to the library supplied.

R. Seynaeve Can the I/O be hidden on the MSP?

J.M. Griffin Yes, in the sense that data can be transferred on the MSP data bus while arithmetic operations are occurring. However, if you call the MSP Library Program to load the internal memory from the host then this is the only program that can be running so it is not hidden.

R. Seynaeve What is the cost of the MSP?

J.M. Griffin The single quantity price is around $10,000.