NOSC SIGNAL PROCESSING EVALUATION LABORATORY

by

Bryson Pennoyer
NAVAL OCEAN SYSTEMS CENTER
San Diego, California, U.S.A.

ABSTRACT A new acoustic Signal Processing Evaluation Laboratory (SPEL) at the Naval Ocean Systems Center (NOSC), San Diego, is described. This laboratory has been designed to support a broad program of research and development of passive and active sonar technology. Full integration of the system allows an analyst to go from multichannel analog tape recorded signals through flexible computer controlled digitization and signal processing such as beamforming, spectral analysis, filtering and detection ending with a high resolution CRT display of the output, all under the control of a central host computer.

The system was designed to provide research analysts an efficient and low cost means to develop and evaluate signal processing concepts, to develop full scale system emulations or simulations and to conduct controlled tests of alternatives through the use of real and simulated data. In addition, the system provides a controlled framework for conducting evaluations of candidate programmable signal processors using real and simulated data. To meet these objectives, the system design capitalizes on the power of new array processor technology and on advanced software concepts to provide the high processing throughput and capability to implement complex processes at a low cost. Combining this technology under the control of a flexible and powerful host computer provides the analyst with an integrated signal processing system.

The principle subsystems of SPEL are the computer controlled 64 channel analog preprocessor, two high-speed signal processors, a PDP-11/70 An overall system design philosophy is presented, and the details of host computer with hardcopy and color and/or black and white CRT displays. the system and subsystems which realize the design philosophy are given.

INTRODUCTION

For the last 10 years, analysts and researchers in the areas of signal processing and display at NOSC have utilized four separate laboratories to conduct their investigations. These were the Acoustic Signal Data Analysis and Conversion System (ASDACS), the Data Acquisition Playback and Analysis (DAPAAN) System, the Display Research Laboratory and the UNIVAC 1108 Computer Center. Each of these systems provided excellent capabilities for the specific tasks for which they were designed, yet had limitations which were a result of the technology of the time. The major deficiency was the lack of integration of the system's capabilities which greatly reduced its efficiency and increased its costs as a result of multiple programming requirements.

Present day signal processing and display requirements benefit greatly from an integrated system which is efficient and provides a low cost means to develop and evaluate signal processing and display concepts. Also needed are capabilities to develop full scale system emulations or simulations and the ability to conduct controlled tests of alternative processing concepts through the use of real and simulated data. Such a system should provide a controlled framework for conducting evaluations of new or alternate programmable signal processors.

The Signal Processing Evaluation Laboratory(SPEL) was designed to meet these objectives. SPEL utilizes the latest technology in signal processing and display equipment and is designed to be expandable to meet future needs.

1. SPEL System Description

As shown in Figure 1, SPEL consists of a unique combination of computer based subsystems that provide analog preprocessing including analog-to-digital conversion, secure ARPANET communications, high-speed signal processing and display research. These subsystems are coupled with a flexible digital computer under the control of multiple users. Data, signal and display processing are easily performed as a result of system integration, a large software library and a broad set of peripheral devices.

1.1 Secure ARPANET Subsystem

The SPEL host computer is a limited server host on the secure ARPANET. The ARPANET is a resource sharing, host-to-host network linking a wide variety of computers at research centers sponsored by Defense Advanced Research Projects Agency (DARPA) and other activities in the continental United States, Hawaii, Norway and England. The secure ARPANET operates on the regular ARPANET using secure message encryption. This secure network links, among others, the NOSC SPEL facility with the Acoustic Research Center (ARC) at Moffett Field, other NOSC facilities and the Naval Research Laboratory in Washington, D.C.

The SPEL link to the ARC offers users full ARPANET protocols including remote terminal operation (TELNET), file transfer (FTP) and message communications (MAILER). Users, both contractor and Navy, have full access to the ARC PDP-10 and hence to the full ARC capabilities via the control routines resident in the PDP-10.

Real data from the ARC data acquisition systems is available on-line to the SPEL facility via transfer of ARC PDP-10 data files. This data can be used to validate processing concepts and systems. Joint experiments, which pool the resources of the ARC, SPEL and others on the secure ARPANET can be conducted. SPEL users will be able to conduct experiments at the ARC with the coordination of a test director.

1.2 Analog Preprocessing Subsystem

Preprocessing capabilities include very flexible multi-channel demultiplexing, amplification and filtering of analog signals, as well as programmable analog-to-digital (A/D) conversion of up to 64 channels. The digital data can be immediately processed in the Raytheon Advanced Digital Signal Processor (ADSP) or temporarily stored on a 300 megabyte random access disk for later transfer to 9 track digital tape or the host computer. Analog-to-digital conversion is performed under computer control using IRIG time code data for starting, stopping and searching the analog tape. Initially, the programmable sections of the system will be manually set. Computer control will be provided in the future. A block diagram of the system is shown in Figure 2.

A wide variety of analog recording formats can be accommodated in the system including IRIG Wideband I, II and III, VIDAR, DAPAAN 9 channel/track and DAPAAN 18 channel/track. Once the analog signal is demultiplexed, it is amplified, anti-alias filtered by a six-pole six-zero elliptic filter and then digitized using one independent programmable A/D converter per channel. Each A/D converter is capable of a 100 kHz conversion rate with 8 or 12 bit resolution. However, the system has a maximum throughput of 500 kHz when the digitized output goes to the ADSP or disk and 50 kHz using magnetic tape. Variations in sample rate caused by tape speed variations are eliminated by using tape recorded reference signals for speed control and for deriving the A/D sample rate.

On-line data analysis ,quality checks, can be made using spectral analysis, crosscorrelation, signal amplitude , and aural tests of the signals to be digitized and are included in the system to improve accuracy and confidence in the converted data.

Digital-to-analog conversion capabilities for up to 28 channels are provided with filtering, amplification and multiplexing of analog data. Digital data input can come from either the 300 megabyte disk or 9 track digital tape. This capability coupled with the power of the signal processors, provides a means of generating analog tapes with known characteristics.

1.3 Signal Processing Subsystem

This subsystem provides the real processing power of SPEL with the extensive signal processing cabapilities of the Raytheon Advanced Digital Signal Processor (ADSP) and the Signal Processing Systems SPS-81. Each processor is programmable by the user through the host computer. These processors provide the important basic signal processing functions of Fast Fourier Transform, digital filtering, quadrature analysis, beamforming, convolution and correlation plus many others. Functions can be used separately for analysis purposes or combined into a total processing system.

SPEL has been designed to readily accommodate additional programmable signal processors by connecting them to the PDP-11/70. This capability can be used for conducting performance tests on selected signal processors or to provide specialized processing capabilities.

1.3.1 Raytheon ADSP

The ADSP is the primary signal processor in the system. It consists of three major components, as shown in Figure 3; 1) the Bus Access Unit to interface external devices to the processor, 2) the Main Memory for program and data storage and 3) the Signal Processing Unit for performing high-speed "number crunching". The ADSP is designed to provide high-speed signal processing and minimize programming costs by providing the following major features:

1. Greatly simplified programming through the elimination of microprogramming and the use of a unique method of dynamically describing data items. Data are characterized via data descriptor (DD) words which contain pertinent information for each variable. The major consequence of using DDs is the separation of structual details of data, i.e. scalar, matrix, real or complex, from the application program. Thus, modifications in data types can be made by simply altering the data descriptors, leaving the application program untouched.

2. A large, high-level, mathematically-oriented signal processing instruction set is incorporated. Future expansion of the instruction set is available through a writable control store memory. Typical instructions are "FFT", which computes the discrete Fourier Transform and "IIR", which performs recursive filtering on a set of data.

3. High speed processing is provided through the combination of a 75 nanosecond system clock and pipelined implementation of data accessing, data formatting and arithmetic computations. In addition, separate buses are provided between memory and the signal processing unit for commands, instructions, and data. The arithmetic is block-floating point (16 bit) two's complement with automatic data scaling. The ADSP can perform 27M multiplies and 53M adds per second simultaneously. A complex

1Ø24 point FFT takes only Ø.84 milliseconds, which includes the application of a data weighting window and bit reversal.

4. A large capacity main memory of 256K 32-bit words, with addressable expansion up to 16 million words, provides the capability of processing relatively large data arrays in memory. Virtual addressing is used to provide easy relocation and context switching.

5. Host computer control is available to allow for execution of the program one step at a time or execution of the total program.

User programs are generated through the use of the signal processing assembler (SPASM) which converts source-level ADSP instructions and data descriptors (DD) to object form. SPASM assigns data to main memory locations and provides linkages from instructions to DDs and from DDs to data.

1.3.2 SPS-81

The SPS-81 is a moderate speed multiprocessor computer designed for signal processing applications. It is composed of an arithmetic processor(AP), an input/output processor (IOP) and a bulk memory of 128K 16-bit words, as shown in Figure 4. The AP handles complex arithmetic and can do 8M multiplies and 12M additions per second simultaneously. The arithmetic is fixed-point (16 bit) two's complement. A complex 1Ø24 point FFT with dynamic scaling of the data typically takes 14 milliseconds.

The SPS-81 is used primarily by means of FORTRAN callable subroutines. Since the machine is entirely microprogrammed, each of these routines may be thought of as causing a load of the appropriate microcode, transmission of data and activation of the SPS-81.

The AP and IOP are separately microprogrammed. Microprogram generation is handled through a cross-assembler called SPASM (not the same as for the ADSP). A utility program called SPUD is available to facilitate program checkout. The resulting microprogram can be initiated by a FORTRAN application routine.

1.4 Host Computer Subsystem

The host computer, a Digital Equipment Corporation PDP-11/7Ø and peripherals, as shown in Figure 5, is the focal point of SPEL and provides multi-user interface and control of the integrated system. A user may proceed from program development and testing to input of data, signal processing, analysis and display using a common set of software and hardware tools.

Computational speed is attained through the use of the floating point processor and the 64Ø kilobytes of high speed (5ØØ nanosecond) MOS memory. The floating point processor provides single and double precision (32 or 64 bit) floating point modes to increase computational accuracy. A double

precision multiplication is performed in 3 microseconds. However, the real computational power of the system is provided by the SPS-81 and Raytheon ADSP signal processors.

Two 300 megabyte disks provide extensive storage for on-line data, programs and the operating system. Additional on-line data storage is available through the use of a 300 megabyte disk which interfaces with the analog preprocessor subsystem. Long term data and program storage is available using either 9 track 800/1600 bpi or 7 track 556/800bpi magnetic tape.

The operating system for the PDP-11/70 is the Programmer's Workbench (PWB)/UNIX system developed by Bell Laboratories. The UNIX time-sharing system is a general-purpose, multi-user, interactive operating system specifically engineered to make the designer's, programmer's, and documenter's computing environment simple, efficient, flexible, and productive. UNIX contains such features as: 1) a hierarchical file system, 2) a flexible, easy-to-use command language, 3) ability to execute sequential, asynchronous and background processes, 4) a powerful context editor, 5) very flexible documentation preparation and text processing system, 6) a high-level programming language called 'C' which is conducive to structured programming, 7) the programming languages BASIC, FORTRAN IV+ and PASCAL, 8) symbolic debugging systems, 9) a variety of system programming tools (e,g. compiler-compilers) and 10) ease of developing device handlers.

The file system consists of a highly-uniform set of directories and files arranged in a tree-like hierarchial structure. Some of the features are: 1) simple and consistent naming conventions, 2)mountable and de-mountable file systems and volumes, 3)file linking across directories, 4)automatic file space allocation and de-allocation that is invisible to the user, 5)a complete set of flexible directory and file protection modes and 6) each physical I/O device, from interactive terminals to main memory, is treated like a file allowing uniform file and device I/O.

1.5 Display Research Subsystem

The display research subsystem is a user oriented laboratory for the analysis and display of digital and video imagery. The laboratory serves as a test site for the development and evaluation of advanced processing and display concepts. In addition, the laboratory, with its controlled environment, is a major resource for human factors research on display formats and perceptual processes.

The laboratory features the high resolution CRT displays and associated processing of the RAMTEK 9400 Display System. This system provides two black and white CRT monitors with 1024x1024 point resolution and 256 levels of intensity and a color monitor with 750x750 point resolution, 4096 colors and 256 levels of intensity. Each monitor can display vectors, conics, bargraphs and raster data in addition to performing pan, zoom, scroll and blink functions. An extensive user library is available for performing image transformations and image processing.

SUMMARY

SPEL is now available at NOSC for the processing of large quantities of analog and digital data. The system can provide real on-line digital data from the Acoustic Research Center by way of the secure ARPANET. Digitized data are also available from an extensive analog library via the analog preprocessor subsystem of SPEL. Signal processing functions are performed in one of two high speed programmable signal processors or in the host computer. Processed data can then be viewed on high resolution color and/or black and white CRT displays, a standard computer line printer or graphic plotter.

The system is intended to serve as a tool for signal and display analysts with special emphasis on ease-of-programming, program development aids, real data access and simulated data generation. It possesses the very high throughput required by the multi- channel, multi-resolution processing problems of future Navy fleet systems.

The system is designed to accommodate new signal processors readily and to provide the means for efficient comparisons of the performance of such devices.

DISCUSSION

F.W. Molino Please give a scenario of how the various signal processors, i.e. TI MVP, SPS-1, will be evaluated? What will you be looking for??

B. Pennoyer The techniques to be used in evaluating the signal processors is the subject of a contract this year. Bench-mark testing using a specific application program and controlled data set will certainly be part of the evaluation.

R. Seynaeve Does the ADSP have provisions to avoid losses of dynamic range after, for example, a multiplication, as the format used is 16-bit block floating point?

B. Pennoyer The multiplication of two 16-bit words results in a 32-bit result with an 8-bit exponent. The 16 most significant bits of the 32 are retained after correction for under or overflow.

R. Seynaeve What is the cost of the ADSP?

B. Pennoyer The cost for future copies of the ADSP has not been firmly established by Raytheon.

Y.S. Wu How long have you worked on this project and how many NOSC people involved?

B. Pennoyer Since 1977; the NOSC project team consists of six in-house people.

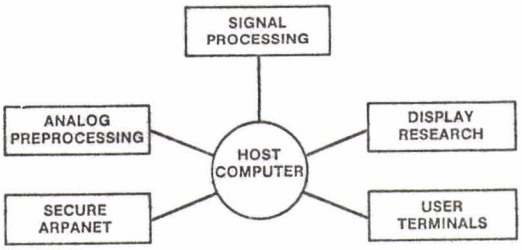

FIG. 1 SPEL CONFIGURATION

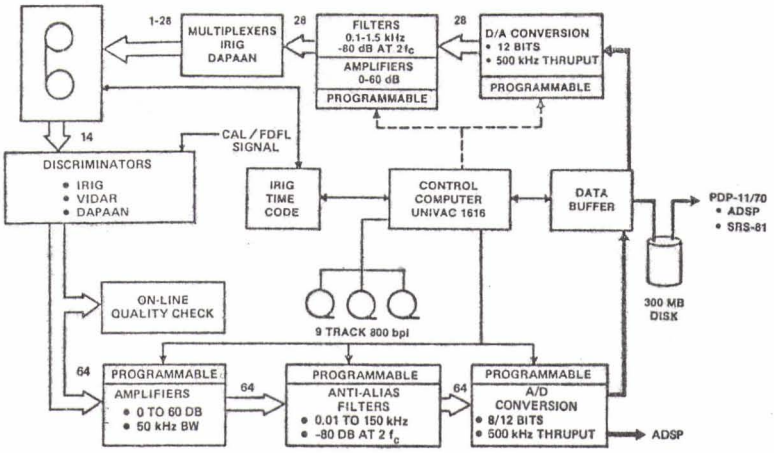

FIG. 2 ANALOG PREPROCESSOR SUBSYSTEM

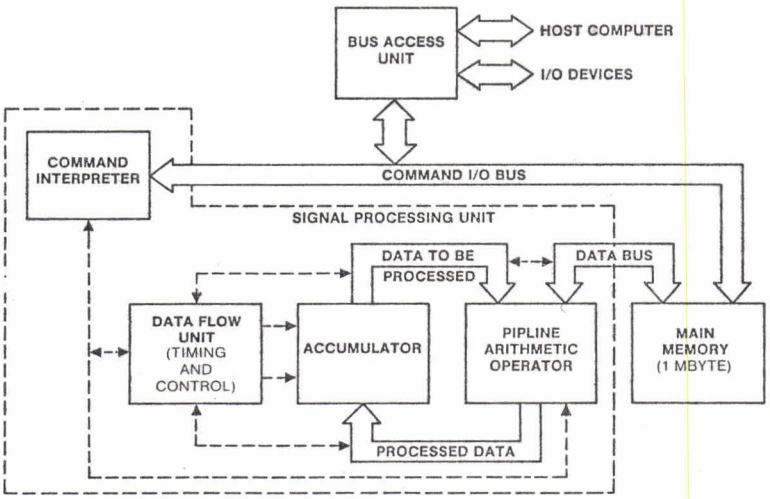

FIG. 3 RAYTHEON ADSP ARCHITECTURE

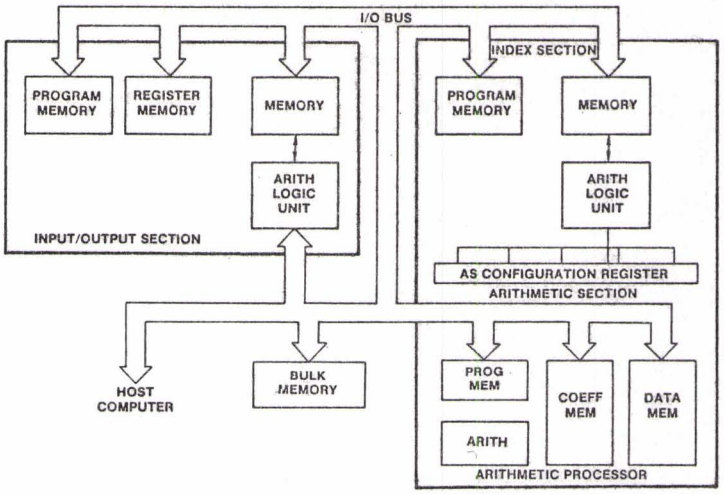

FIG. 4 SPS-81 ARCHITECTURE

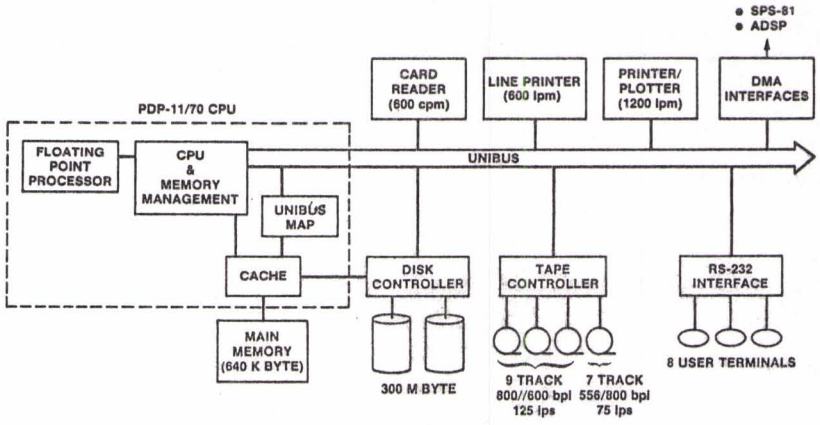

FIG. 5 HOST COMPUTER SUBSYSTEM